CLOCK REGENERATION CIRCUIT

Patent number: EP0989706
Publication date: 2000-03-29
Inventor: SHIRAISHI KENICHI (JP); TADA SHUNICHI (JP)
Applicant: KENWOOD CORP (JP)
Classification:
- International: H04L27/22; H04J9/00
- european: H04L27/06C, H04J9/00, H04L7/06
Application number: EP19980924555 19980610
Priority number(s): WO1998JP02553 19980610; JP19970171184 19970613; JP19970201036 19970711

Also published as:
WO9857470 (A1)

Abstract of **EP0989706**

A clock regeneration circuit for regenerating a clock signal for demodulating data from an AM data multiplex modulated signal where digitally modulated signals are multiplexed in the same frequency band as those of an amplitude-modulated signal at the same time. The carrier for an amplitude-modulated signal is extracted from an AM data multiplex modulated signal where digitally modulated signals are multiplexed in the same frequency band as those of the amplitude-modulated signal at the same time through a band-pass filter (1), and the oscillation frequency of a voltage-controlled oscillator (5) is controlled by the output of a phase comparator (3) through a loop filter (4). The oscillation output of the voltage-controlled oscillator (5) is supplied to a direct digital synthesizer (6) and the phase of the carrier extracted through the band-pass filter (1) is compared with the phase of the output of the direct digital synthesizer (6) by means of the phase comparator (3). The oscillation output of the voltage-controlled oscillator (5) is then synchronized with the carrier for the amplitude-modulated signal to produce a clock signal for demodulating data.

FIG. 1